IN THE CLAIMS

1. (currently amended) A method of fabricating an integrated circuit seal ring comprising:

providing an active area including semiconductor device structures; and

forming a continuous conductive loop around the perimeter of said integrated circuit wherein said conductive loop has a plurality of sections having at least two different alternating widths wherein each of said sections has a different width from its adjacent sections wherein characteristic impedance of each of said two different widths is different, wherein said conductive loop forms said seal ring.

2. (original) The method according to Claim 1 wherein the narrowest of said different alternating widths is between about 0.5 and 50 μm.

3. (original) The method according to Claim 1 wherein the widest of said different alternating widths is between about 1 and 55 μm.

4. (canceled)

5. (previously presented) A method of fabricating an integrated circuit seal ring comprising:

providing an active area including semiconductor device structures; and

forming a continuous conductive loop around the perimeter of said integrated circuit by patterning and forming a plurality of stacked, interconnected, conductive layers wherein said conductive loop has a plurality of sections having at least two different alternating widths, wherein said conductive loop forms said seal ring.

6. (original) The method according to Claim 5 wherein the narrowest of said different alternating widths is between about 0.5 and 50 μm.

7. (original) The method according to Claim 5 wherein the widest of said different alternating widths is between about 1 and 55 μm.

8. (original) The method according to Claim 5 whereby the characteristic impedance of each of said different alternating widths is different.

9. (original) A method of fabricating an integrated circuit seal ring comprising:

providing an active area including semiconductor device structures; and

forming a continuous conductive loop around the perimeter of said integrated circuit by patterning and forming a plurality of stacked, interconnected, conductive layers whereby said conductive loop has a plurality of sections having at least two different alternating widths and each of said conductive layers is formed by steps comprising:

depositing an inter-metal dielectric layer;

etching openings through said inter-metal dielectric layer;

filling said openings with a conductive via layer; and

depositing and patterning a conductive metal layer to make contact to said conductive via layer filling said openings in said inter-metal dielectric layer,

wherein a first of said conductive via layers makes electrical contact to signal ground points within the substrate of said active area, and wherein each of subsequent said

conductive via layers makes electrical contact to previous patterned said conductive metal layer, completing fabrication of said integrated circuit seal ring.

10. (original) The method according to Claim 9 wherein the narrowest of said different alternating widths is between about 0.5 and 50 μm.

11. (original) The method according to Claim 9 wherein the widest of said different alternating widths is between about 1 and 55 μm.

12. (original) The method according to Claim 9 whereby the characteristic impedance of each of said different alternating widths is different.

13-23. (canceled)

24. (previously presented) A method of fabricating an integrated circuit seal ring comprising:

providing an active area including semiconductor device structures; and

forming a continuous conductive loop around the perimeter of said integrated circuit by forming and patterning a plurality of stacked, interconnected, conductive layers wherein said conductive loop has a plurality of sections having at least two different alternating widths wherein each of said different alternating widths has a different characteristic impedance, wherein said conductive loop forms said seal ring.

25. (previously presented) The method according to Claim 24 wherein the narrowest of said different alternating widths is between about 0.5 and 50 μm.

26. (previously presented) The method according to Claim 24 wherein the widest of said different alternating widths is between about 1 and 55 μm.